THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LOUIS LU-CHEN HSU,
CHANG-MING HSIEH, LYNDON R. LOGAN,
JACK A. MANDELMAN,
and SEIKI OGURA

Appeal No. 1997-3162
Application 08/540,961[1]

ON BRIEF

Before BARRETT, FLEMING, and LALL, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

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[1] Application for patent filed October 11, 1995, entitled "Method To Suppress Subthreshold Leakage Due to Sharp Isolation Corners In Submicron FET Structures," which is a continuation of Application 08/274,055, filed July 12, 1994, now abandoned.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 18, 2, and 3.

We reverse.

BACKGROUND

The invention relates to a field effect transistor utilizing shallow trench isolation and a gate structure for such a transistor which mitigates leakage current induced along the edges of the device.

Claim 18 is reproduced below.

> 18. A field effect transistor isolated by shallow trench isolation devoid of local oxidation of silicon (LOCOS) isolation, said shallow trench isolation having a channel width between first and second shallow trenches at first and second shallow trench edges and a gate which extends across said channel width between said first and second shallow trenches, said gate having a first length at said shallow trench edges and a second length less than said first length between said shallow trench edges, said first length and said second length being related such that a threshold voltage, V_t, at said shallow trench edges is substantially equal to V_t between said shallow trench edges.

The Examiner relies on the following prior art:

Shimizu et al. (Shimizu) 5,466,623 November 14, 1995
(effective filing date June 30, 1988)

Kikuchi[2] 4-207763 March 4, 1994
(Japanese Unexamined Published Patent Application (Kokai))

Kikuchi discusses the prior art in connection with figure 4, which teaches providing a gate electrode pattern 3 across an active source-drain diffusion region 5, 6 surrounded by LOCOS-type isolating-insulating film 2. Such a transistor has two problems (translation, page 3): (1) the actual channel width L2 at the end of the active region is narrower than the actual channel width L1 at the center of the active region due to faster diffusion of the layers 5, 6 because of oxidation stresses, which causes the electric field to become concentrated and causes leakage current and a short circuit between the source and drain due to punch-through; and (2) the pattern width of the silicon pattern is narrower at the end of the gate area 3c, lead area 3b, and protrusion area 3d than at the center of the gate area 3c due to the difference in exposure caused by the difference in height of the film 2, which causes the channel width to be narrow and may cause the

[2] Our understanding of Kikuchi is based on a translation prepared by the Patent and Trademark Office, a copy of which accompanies this decision.

pattern 3 to be discontinuous. Kikuchi overcomes the problems by making the pattern width L3 of the contact formation area 13a, the pattern width L4 of the lead area 13b, and the pattern width L6 of the protrusion area 13d wider than the pattern width L5 of the gate area 13c (translation, page 5).

Shimizu discloses that trench isolation is an alternative to the conventional LOCOS isolation method (col. 2, lines 30-35). Trench isolation has several disadvantages which prevent it from being widely used (col. 2, line 67 to col. 3, line 20).

Claims 18, 2, and 3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kikuchi and Shimizu.

We refer to the Final Rejection (Paper No. 18) and the Examiner's Answer (Paper No. 25) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 23) (pages referred to as "Br__") and the Reply Brief (Paper No. 26) (pages referred to as "RBr__") for a statement of Appellants' arguments thereagainst.

OPINION

Kikuchi discloses a gate structure having widened portions where it crosses over the edge of the surrounding

LOCOS isolation region. We understand the Examiner's position that Kikuchi's gate structure is exactly the same as Appellants' gate structure. The issues are: (1) whether it would have been obvious to use this gate structure with a surrounding shallow trench isolation instead of LOCOS isolation; and, if so, (2) whether it would have been obvious to select the lengths "such that a threshold voltage, V_t, at said shallow trench edges is substantially equal to V_t between said shallow trench edges," as claimed.

The Examiner's sole motivation for modifying Kikuchi to use trench isolation is the finding that Shimizu teaches that trench isolation is better than LOCOS (EA3). Appellants argue that Shimizu discloses that while trench isolation solves certain difficulties associated with the conventional LOCOS isolation method, it explains that trench isolation has problems with edge sidewall leakage, among other things, and therefore ultimately indicates that trench isolation is inferior to LOCOS (Br8). As Appellants note (Br8-9), Shimizu implements the invention with non-trench isolation.

The relative weight of the advantages versus disadvantages of trench isolation, i.e., whether trench

isolation is "better" than LOCOS isolation, is not considered determinative. Something may be obvious even if has disadvantages. What is important is whether one of ordinary skill in the art would have sought to use the widened gate structure of Kikuchi if the surrounding LOCOS isolation was replaced with shallow trench isolation. The Examiner's bare conclusion that it would have been obvious to mechanically substitute trench isolation for the LOCOS isolation fails to address whether the problems solved by Kikuchi would have existed with trench isolation and, therefore, would have suggested applying Kikuchi's solution.

Trench isolation is produced by etching (Shimizu, col. 2, lines 40-45) and, thus, would not produce the oxidation stresses of LOCOS leading to the first problem described in Kikuchi (translation, page 3). Trench isolation has a planar surface (Shimizu, col. 2, lines 55-59; figure 3E) and, thus, would not produce overexposure of the ends of the gate due to the height difference of the LOCOS isolation above the active region leading to the second problem described in Kikuchi (translation, page 3). Accordingly, we do not find any evidence why one of ordinary skill in the art would have been

motivated to use the widened gate structure of Kikuchi if the surrounding LOCOS isolation was replaced with shallow trench isolation. For this reason, we conclude that the Examiner has failed to establish a prima facie case of obviousness.

In addition, as to the second issue, we disagree with the following statements by the Examiner (EA3): "Any inherent threshold voltage, V_t, at the shallow trench edges is obviously substantially equal to V_t between the shallow trench edge. Note that 'substantially equal' does not mean 'equal'."

It is true that "substantially equal" does require exact equality. Nevertheless, "substantially equal" is not without meaning and does not imply that any two voltages will do. The voltages must be approximately equal and we agree with Appellants' argument (at RBr2) that the voltages must be sufficiently close to meet the functional requirement of avoiding the prior art leakage current problems or at least minimize it to the point that it does not adversely affect device performance. There is no evidence that applying the gate structure of Kikuchi to a trench isolation structure would "inherently" have the desired relationship. Kikuchi does not disclose any relationship between the gate length and

the threshold voltage. For this additional reason, we conclude that the Examiner has failed to establish a prima facie case of obviousness.

For the two reasons discussed above, the rejection of claims 18, 2, and 3 is reversed.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
PARSHOTAM S. LALL Administrative Patent Judge	)	

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